AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings includes changes to add the legend "Conventional Art" to Figures 6-10.

REMARKS

Claims 1-13 are pending in the above application. By the above amendment claims 8-13 have been added.

The Office Action dated February 2, 2007, has been received and carefully reviewed. Each issue raised in that Office Action is addressed below, and reconsideration and allowance of claims 1-13 is respectfully requested in view of the following remarks.

DRAWING OBJECTIONS

Figures 6-10 were objected to for failing to include a legend such as "Prior Art." Submitted herewith are replacement Figures 6-10 which are now labeled "Conventional Art" to address this objection.

The basis for objecting to the reference numerals in the figures is unclear. While Figures 1-5 include some elements similar to some elements of Figures 6-10, these elements are not necessarily identical to the elements found in the conventional art drawings. Therefore, one set of reference numerals has been used to identify elements of a conventional device and another set of reference numerals has been used to identify elements of the present invention. Reference numeral 1 in Figure 1 and reference numeral 301 in Figure 6 both designate antennas, but not the same antenna. This is not an instance of different reference numerals being used to designate the same part as prohibited by 37 C.F.R. 1.84(p)(4). It is therefore believed that the drawings comply with the requirements of 37 C.F.R. 1.84, and the withdrawal of the drawing objection is respectfully requested.

CLAIM OBJECTIONS

Claim 3 was objected to for reciting a gain switching detection circuit which was previously recited in claim 1. The limitation of a gain switching detection circuit has been removed from claim 1 by the above amendment. It is believed that this amendment to claim 1 and the further changes to claim 3 obviate the objection to claim 3.

REJECTIONS UNDER 35 U.S.C. 112, FIRST PARAGRAPH

Claim 1 is rejected under 35 U.S.C. 112, first paragraph, because it is asserted that the recited "at least one gain switching detection circuit" is not sufficiently disclosed. By the above amendment, this limitation has been removed from claim 1. It is believed that this amendment to claim 1 addresses the rejection under 35 U.S.C. 112, first paragraph.

REJECTIONS UNDER 35 U.S.C. 103(a)

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over the art discussed in the background section of the application (hereinafter the "Background Art") in view of Eliezer and further in view of Mano. It is respectfully submitted that a proper motivation for modifying the references has not been provided and that therefore a prima facie case of obviousness has not been presented. Moreover, even if the references could be combined, the result would not be the invention recited in claim 1. Each of these issues is discussed below.

As provided by MPEP 706.02(j), one of the showings needed to support a rejection under 35 U.S.C. 103(a) is an identification of the "proposed modification of an applied reference(s) necessary to arrive at the claimed subject matter." In the present case, the Office Action merely indicates that the teaching of Mano should be added to the Background Art "for the benefit of controlling or keeping track of the sequencing of activities in a digital system." It is not clear what activities in the Background Art the examiner is proposing to "control" or "keep track of" based on the teachings of Mano or that any such activities require control or tracking that is not already provided by the Background Art. It is also not clear how Mano, which is little more than a definition of "counter," would motivate one to add a counter in some manner to the Background Art. It is therefore respectfully submitted that a proper motivation for modifying the Background Art has not been provided and that claim 1 is therefore allowable over the art of record.

If this rejection is maintained, it is respectfully requested that the examiner identify the change to the Background Art that is being proposed, what in the Background Art needs to be tracked or controlled in some manner, and how the disclosure of Mano suggests such a modification to one skilled in the relevant arts.

Furthermore, even if a motivation for modifying the Background Art were provided, the result would still not be the invention of claim 1. Claim 1 recites a receiving apparatus comprising, inter alia, a counter circuit. The Background Art does not disclose a counter circuit; Eliezer does not disclose a counter circuit. The fact that a "counter can be found inside a processor" does not establish that a counter is present in the Background Art or in Elieser. If the examiner intends to rely on an inherency argument to show the presence of a counter in Elieser, it is respectfully submitted that the requirements of MPEP 2112 have not been satisfied. The record does not show that a counter is "necessarily present" in Elieser; the fact that a counter might be present in Elieser does not establish inherency. For this reason as well, it is respectfully submitted that the art of record does not show each element recited by claim 1, and that claim 1 is allowable over the art of record.

Claims 2-7 depend from claim 1 and are submitted to be allowable for at least the same reasons as claim 1.

Claim 5 further distinguishes over the art of record by reciting additional details of the claimed binarizing circuit. Claim 5 recites, for example, that the binarizing circuit of claim 1 includes at least one minimum value detection circuit and at least one maximum value detection circuit accepting input of at least one demodulated signal from said at least one demodulator by way of at least one demodulated signal holding circuit. The art of record does not show or suggest minimum or maximum value detection circuits receiving a demodulated signal from a demodulator by way of at least one demodulated signal holding circuit as recited in claim 5. Claim 5 further distinguishes over the art of record for this reason.

Claim 6 further distinguishes over the references of record by reciting that the claimed binarizing circuit includes, inter alia, at least one offset canceler circuit and at least one offset canceler output holding circuit. The Background Art shows an offset canceler, but Eliezer and Mano do not show or suggest an offset canceller output holding circuit. These references therefore also in no manner suggest providing at least one offset canceler output holding circuit as recited in claim 6.

The Office Action seems to suggest that Eliezer's hold control somehow suggests an offset canceler output holding circuit because "this unit is considered to be functional equivalent

to the holding circuit disclosed in Eliezer." However, it is not clear how Eliezer's adaptive data slicer in any manner suggests a change to an offset canceler. Even if it the above statement is assumed, for sake of argument only, to be true, the Background Art and Eliezer in no manner suggest any structures for performing "equivalent" functions. The test for obviousness is not whether two structures perform equivalent functions but whether one skilled in the relevant arts would have found it obvious to make the claimed invention based on the teachings of the prior art. Nothing in the record suggests that one skilled in the art would have found it obvious to modify the Background Art and Eliezer to produce a device having an offset canceler output holding circuit, and claim 6 is submitted to distinguish over the art of record for this reason as well.

New claim 8 is also submitted to be allowable over the art of record. Claim 8 recites a counter circuit receiving a first input when a comparing circuit outputs a positive gain setting signal and a second input when the comparing circuit outputs a negative gain setting signal, the counter circuit being operatively connected to the slice level holding circuit. The art of record in no manner shows or suggests a counter circuit receiving first and second inputs as claimed or a counter circuit operatively connected to a slice level holding circuit as claimed. Claim 8 further recites that the counter circuit causes the slice level holding circuit to hold the slice level at a substantially constant value for a given time when the first input changes to the second input or when the second input changes to the first input. A counter circuit holding a slice level circuit at a given level as recited in this claim is also not shown or suggested by the art of record. Claim 8 is submitted to be allowable for at least this reason.

Claims 9 and 10 depend from claim 8 and are submitted to be allowable for at least the same reasons as claim 8.

Claim 11 is submitted to be allowable over the art of record for at least the reasons provided above in connection with claim 1. In addition, claim 11 recites means for holding a slice level employed by a binarizing circuit at a substantially constant value. The art of record does not show "means for holding" as recited in claim 11 or any structure equivalent to the means for holding disclosed in the specification. See, e.g. MPEP 2183. Claim 11 is submitted to further distinguish over the art of record for at least this reason.

Claims 12 and 13 depend from claim 11 and are submitted to be allowable for at least the same reasons as claim 11.

CONCLUSION

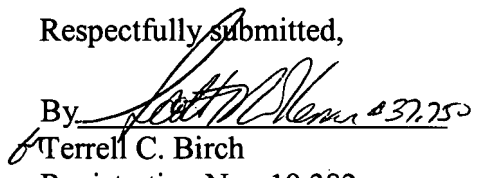
Each issue raised in the Office Action dated February 2, 2007, has been addressed, and it is believed that claims 1-13 are in condition for allowance. Wherefore, reconsideration and allowance of these claims is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the examiner is respectfully requested to contact Scott Wakeman (Reg. No. 37,750) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.14; particularly, extension of time fees.

Dated: April 27, 2007

Respectfully submitted,

By 

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